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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,989	07/30/2003	Richard W. Adkisson	200207724-1	9148

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,989	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *26-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-14* is/are rejected.

7)☒ Claim(s) *4-11 and 15-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *073003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment dated 3/22/06.

2. Claims 1-22 are presented for examination. Applicant has canceled claims 23-31.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaskins et al., U.S. Patent 6,161,188.

5. Regarding claim 1, a system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal (output of selective clock multiplier 410) and said bus clock domain is operable with a bus clock signal (wherein the bus clock signal is BCLK 411), said core and bus clock signals having a ratio, comprising:

a. means disposed in a bus clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals (not explicitly shown but inter-controller clock relationship control signals 412-414 of Gaskins are inherently generated, col. 9, line 66 through col. 10, line 6 and figure 4); and

b. means disposed in a core clock synchronizer controller portion operating responsive to said set of inter-controller clock relationship control signals for synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal (generates a core clock signal based ratio of bus clock, col. 9, line 66 through col. 10, line 6 and figure 4).

6. Regarding claim 12, Gaskins taught the claimed system therefore he also teaches the claimed method.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins et al., U.S. Patent 6,161,188 in view of Magro et al., 6,516,362.

9. Regarding claim 2, Gaskins taught the system according to claim 1, as described above. Gaskins does not explicitly disclose wherein said means disposed in said bus clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals is operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

Magro teaches a means disposed in a clock synchronizer controller portion (synchronizer logic 202) for generating a set of inter-controller clock relationship control signals is operable

responsive to a SYNC pulse (phase_sync signal 206) that is sampled in a clock domain by a clock signal (figures 3A, 3B and col. 8, lines 6-14). The invention of Magro is in the same field endeavor as that of Gaskins in that they are both directed toward communicating data between two different clock domains. Magro further provide an advantage of identifying a correct clock edge on which to launch or assert a signal the correct edge sample from a bus.

It would have been obvious to one of ordinary skill in the art, having the teachings of Gaskins and Magro before the at the time of the invention, to modify the bus clock synchronizer controller of Gaskins to generate the control signal as taught by Gaskins responsive to a SYNC pulse as taught by Magro.

One of ordinary skill in the art would have been motivated to make the modification in order to achieve the advantage of identifying a correct clock edge on which to launch or assert a signal the correct edge sample from a bus

10. Regarding claim 13, Gaskins taught the claimed system therefore he also teaches the claimed method.

11. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins et al., U.S. Patent 6,161,188 and Magro et al., 6,516,362 in further view of Grey, "Analysis and Design of Analog Integrated Circuits".

12. Regarding claim 14, Gaskins together with Magro taught the system according to claim 2, as described above. Magro further teaches wherein said SYNC pulse is generated when a rising edge in said core clock signal (CLK_CPU, figure 3b) is at least substantially coincident with a rising edge in said bus clock signal (CLK_MEM, figure 3b).

However Gaskins together with Magro do not explicitly disclose wherein the SYNC pulse is generated by a phase-locked loop (PLL).

Grey teaches PLL may be used to generate pulses (section 10.4). Further, Grey further teaches that PLLs are particularly amenable to monolithic construction and can be fabricated at low cost. It appears that feature of using a PLL in Grey provides the advantages of using very little space with low cost.

It would have been obvious to one of ordinary skill in the art, having the teachings of Gaskins, Magro and Grey before them at the time the invention was made to modify the SYNC pulse of Magro to be generated by a PLL as taught by Grey.

One of ordinary skill in the art would have been motivated to make this modification in order to obtain the advantages of using very little space with low cost.

Allowable Subject Matter

13. Claims 4-11 and 15-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest individually or in combination the system further comprises wherein said means disposed in said core clock synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,157,233 to Horigan et al. teaches a system that determines the ratio of a bus clock to a core clock.

U.S. Pat. App. Pub. No. US 2003/0188083 to Kumar et al. teaches a system that derives a core clock based on a bus clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James K. Trujillo
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Technology Center 2100